WHAT IS CLAIMED IS:

1. A processor synchronous with an instruction clock signal, comprising:

an execution control unit synchronous with the instruction clock signal and operable to execute an instruction per clock cycle of the instruction clock signal;

an input pipeline unit synchronous with the instruction clock signal and operable to receive a stream of input data words one data word per clock cycle of the instruction clock signal, the input pipeline unit further operable to selectively output one input data word per clock cycle of the instruction clock signal;

a data modify unit coupled to the input pipeline unit, the data modify unit operable to selectively modify input data words received form the input pipeline unit according to instruction-specified operators to generate modified data words one modified data word per clock cycle of the instruction clock signal; and

a processor output selector operable to selectively output, at each clock cycle of the instruction clock signal, an instruction-specified one of the input data words and the modified data words.

2. The processor of claim 1, further comprising:

a data compare unit coupled to the input pipeline unit, the data compare unit operable to selectively compare input data words received from the input pipeline unit to instruction-specified operands to generate compare flags.

3. The processor of claim 2, wherein the execution control unit is operable to configure during each clock cycle of the instruction clock signal at least one of the data modify unit and the data compare unit according to a current instruction.

4. The processor of claim 3, wherein the execution control unit is operable to determine a next instruction to be processed according to compare flags generated by the data compare unit during a current clock cycle of the instruction clock signal and a branch operator specified in the current instruction.

5. The processor of claim 2, wherein the input pipeline unit comprises:

a plurality of successive stages each having an output, each respective stage operable to output a respective one of the input data words after a delay of a number of clock cycles of the instruction clock signal corresponding to a position of the respective stage in the input pipeline unit; and

an output multiplexer coupled to at least a subset of the stages of the input pipeline unit, the output multiplexer operable to select for output to the data modifying unit and the data compare unit an instruction-specified one of the outputs from the subset of the stages of the input pipeline unit.

6. The processor of claim 2, further comprising:

a register bank accessible by the execution control unit, the data compare unit and the data modify unit, the register bank operable to store data for the execution control unit, the data compare unit and the data modify unit; and

a peripheral unit accessible by the data modify unit, the peripheral unit for storing instruction-specified data therein.

7. The processor of claim 2, wherein the processor output selector comprises a multiplexer coupled to the input pipeline unit and the data modify unit to receive, respectively, the input data words and the modified data words.

8. The processor of claim 2, wherein the data modify unit comprises arithmetic logic units operable to perform instruction-specified operations on the input data words.

9. The processor of claim 1, wherein the execution control unit is operable to execute one instruction having at least two branch control operators during each clock cycle of the instruction clock signal.

10. The processor of claim 1, wherein the execution control unit is operable to execute one conditional instruction during each clock cycle of the instruction clock signal.

11. The processor of claim 1, wherein the execution control unit is operable to repeat execution of a current instruction having a background mode operator during a next clock cycle of the instruction clock signal.

12. A processor synchronous with an instruction clock signal, comprising:

an execution control unit synchronous with the instruction clock signal and operable to execute an instruction per clock cycle of the instruction clock signal;

an input pipeline unit synchronous with the instruction clock signal and operable to receive a stream of input data words one data word per clock cycle of the instruction clock

signal, the input pipeline unit further operable to selectively output the input data words one input data word per clock cycle of the instruction clock signal; and

a data compare unit coupled to the input pipeline unit, the data compare unit operable to generate compare flags by selectively comparing input data words received from the input pipeline unit to instruction-specified operands,

wherein the execution control unit is operable to determine a next instruction to be processed according to compare flags generated by the data compare unit during a current clock cycle of the instruction clock signal and a branch operator specified in a current instruction.

13. A processor synchronous with an instruction clock signal, the processor comprising:

an input pipeline unit operable to receive a plurality of input data words at a rate of one input data word per clock cycle of the instruction clock signal;

an execution control unit;

an instruction memory storing instructions for execution by the execution control unit,

wherein the execution control unit is operable to execute, during each clock cycle of the instruction clock signal, one of the instructions so as to control an instruction-specified operation on an instruction-specified one of the input data words in the input pipeline unit.

14. The processor of claim 13, further comprising:

a data modify unit coupled to the input pipeline unit, the data modify unit operable to selectively modify, during each clock cycle of the instruction clock signal, an input data word received from the input pipeline unit in accordance with an instruction specified operator, the data modify unit further operable to generate a modified output data word.

15. The processor of claim 14, further comprising:

a data compare unit coupled to the input pipeline unit, the data compare unit operable to selectively compare during each clock cycle of the instruction clock signal an input data word received from the input pipeline unit with an instruction specified operand and generating a resultant set of compare flags.

16. The processor of claim 15, wherein the execution control unit is operable to configure, during each clock cycle of the instruction clock signal, at least one of the data modify unit and the data compare unit in accordance with a current instruction.

17. The processor of claim 16, wherein the execution control unit is operable to determine a next instruction to be executed in accordance with the compare flags generated by the data compare unit in a current clock cycle of the instruction clock signal and a branch control operator in the current instruction.

18. The processor of claim 13, wherein the input pipeline unit comprises:

a plurality of successive stages each having an output, each respective stage outputting a respective one of the input data words after a delay of a number of clock cycles of the instruction clock signal corresponding to a position of the respective stage in the input pipeline unit; and

an output multiplexer coupled to at least a subset of the stages of the input pipeline unit, the output multiplexer operable to select for output to the data modifying unit an instruction-specified one of the outputs from the subset of the stages of the input pipeline unit.

19. The processor of claim 14, further comprising a processor output selector coupled to the input pipeline unit and the data modify unit, the processor output selector operable to selectively output, at each clock cycle of the instruction clock signal, one of the input data words and the modified data words.

20. The processor of claim 15, further comprising:

a register bank accessible by the execution control unit, the data compare unit and the data modify unit, the register bank operable to store data for the execution control unit, the data compare unit and the data modify unit; and

a peripheral unit accessible by the data modify unit, the peripheral unit for storing instruction-specified data therein.

21. The processor of claim 14, wherein the data modify unit comprises arithmetic logic units operable to perform instruction-specified operations on the input data words.

22. The processor of claim 13, wherein the execution control unit is operable to execute one instruction having at least two branch control operators during each clock cycle of the instruction clock signal.

23. The processor of claim 13, wherein the execution control unit is operable to execute one conditional instruction during each clock cycle of the instruction clock signal.

24. The processor of claim 13, wherein the execution control unit is operable to repeat execution of a current instruction having a background mode operator during a next clock cycle of the instruction clock signal.

25. A processor synchronous with an instruction clock signal, comprising:

an input pipeline unit operable to continuously receive a stream of input data words including one data word during each clock cycle of the instruction clock signal, the input pipeline unit further operable to output successive ones of the data words during successive clock cycles of the instruction clock signal;

a data modify unit coupled to the input pipeline unit, said data modify unit operable to selectively modify during each clock cycle of the instruction clock signal an input data word received from the input pipeline unit in accordance with an instruction specified operator and generating a resultant output data word;

a data compare unit coupled to the input pipeline unit, said data compare unit operable to selectively compare during each clock cycle of the instruction clock signal an input data word received from the input pipeline unit with an instruction specified operand and generating a resultant set of compare flags; and

an execution control unit, coupled to the data modify unit and data compare unit, the execution control unit operable to configure during each clock cycle of the instruction clock signal at least one of the data modify unit and the data compare unit in accordance with a current instruction.

26. The processor of claim 25, the execution control unit operable to determine a next instruction to be processed by the execution control unit in accordance with the compare flags generated during a current clock cycle of the instruction clock signal and a branch control operator in the current instruction.

27. The processor of claim 25, wherein the input pipeline unit comprises:

a plurality of successive stages each having an output, each respective stage operable to output a respective one of the input data words after a delay of a number of clock cycles of the instruction clock signal corresponding to a position of the respective stage in the input pipeline unit; and

an output multiplexer coupled to at least a subset of the stages of the input pipeline unit, the output multiplexer operable to select for output to the data modifying unit an instruction-specified one of the outputs from the subset of the stages of the input pipeline unit.

28. The processor of claim 27, wherein the output multiplexer is operable to select for output to the data compare unit an instruction-specified one of the outputs from the subset of the stages of the input pipeline unit.

29. The processor of claim 25, wherein the input pipeline unit comprises:

first and second input pipelines, each pipeline having a plurality of successive stages each having an output, each respective stage operable to output a respective input data word of a first stream and a second stream of input data words after a delay of a number of clock cycles of the instruction clock signal corresponding to a position of the respective stage in the input pipeline unit;

a first output multiplexer coupled to at least a first subset of the stages of the first input pipeline, the first output multiplexer operable to select for output to the data modify unit an instruction-specified one of the outputs from the first subset of the stages of the first input pipeline; and

a second output multiplexer coupled to at least a second subset of the stages of the second pipeline, the second output multiplexer operable to select for output to the data modify unit an instruction-specified one of the outputs from the second subset of the stages of the second input pipeline.

30. The processor of claim 29, further comprising:

a register bank accessible by the execution control unit, the data compare unit and the data modify unit, the register bank storing data for the execution control unit, the data compare unit and the data modify unit; and

a peripheral unit accessible by the data modify unit, the peripheral unit for storing instruction-specified data therein.

31. The processor of claim 30, wherein the data modify unit comprises:

a first input multiplexer coupled to the first and second output multiplexers of the input pipeline unit, the register bank and the peripheral unit, the first input multiplexer operable to selectively receive data from an instruction-specified one of the first and second output multiplexers, a memory location of the register bank and a memory location of the peripheral unit; and

a second input multiplexer coupled to the first and second output multiplexers of the input pipeline unit, the register bank and the peripheral unit, the second input multiplexer operable to selectively receive data from an instruction-specified one of the first and second

output multiplexers, a memory location of the register bank and a memory location of the peripheral unit.

32. The processor of claim 31, wherein the data modify unit comprises:

a first arithmetic logic unit coupled to the output of the first input multiplexer of the data modify unit, the first arithmetic logic unit selectively performing an instruction-specified operation on data provided by the first input multiplexer of the data modify unit; and

a second arithmetic logic unit coupled the output of the second input multiplexer of the data modify unit, the second arithmetic logic unit selectively performing an instruction-specified operation on data provided by the second input multiplexer of the data modify unit.

33. The processor of claim 32, wherein the data modify unit comprises:

a third arithmetic logic unit coupled to the outputs of the first and second arithmetic logic units, the third arithmetic logic unit performing an instruction-specified operation on data provided by outputs of the first and second arithmetic logic units.

34. The processor of claim 33, wherein the input pipeline unit comprises:

first and second pass-through pipelines, each pipeline having a plurality of successive stages each having an output, each respective stage outputting a respective input data word of the first and second streams of input data words after a delay of a number of clock cycles of the instruction clock signal corresponding to a position of the respective stage in the input pipeline unit;

a third output multiplexer coupled to at least a third subset of the stages of the first pass-through pipeline, the third output multiplexer operable to select for output to the data modify unit an instruction-specified one of the outputs from the third subset of the stages of the first pass-through pipeline; and

a fourth output multiplexer coupled to at least a fourth subset of the stages of the second pass-through pipeline, the fourth output multiplexer operable to select for output to the data modify unit an instruction-specified one of the outputs from the fourth subset of the stages of the second pass-through pipeline.

35. The processor of claim 34, wherein the data modify unit comprises:

a first data modify unit output multiplexer coupled to outputs of the first and third arithmetic logic units, and coupled to outputs of the third and fourth output multiplexers of

the input pipeline unit, the first data modify unit output multiplexer operable to select for output an instruction-specified one of the outputs of the first and third arithmetic logic units and the outputs of the third and fourth output multiplexers of the input pipeline unit; and

a second data modify unit output multiplexer coupled to outputs of the second and third arithmetic logic units, and coupled to outputs of the third and fourth output multplexers of the input pipeline unit, the second data modify unit output multiplexer operable to select for output an instruction-specified one of the outputs of the second and third arithmetic logic units and the outputs of the third and fourth output multiplexers of the input pipeline unit.

36. The processor of claim 30, wherein the data compare unit comprises:

a plurality of source select and mask units, each source select and mask unit operable to select as mask operands instruction-specified ones of the outputs of the first and second output multiplexers of the input pipeline unit, an output of the register bank, an output of the peripheral unit, and an immediate data output of the execution control unit, each source select and mask unit generating a masked output;

each source select and mask unit operable to select as compare operands instruction-specified ones of the outputs of the first and second output multiplexers of the input pipeline unit, an output of the register bank, an output of the execution control unit and an immediate data output of the execution control unit, each source select and mask unit generating a compare output; and

a plurality of comparators coupled to the outputs of the source select and mask units, the comparators generating compare results of comparing the masked outputs and the compare outputs of the source select and mask units.

37. The processor of claim 36, wherein the data compare unit comprises:

a plurality of flag update units coupled to the outputs of the comparators, the flag update units performing an instruction-specified logic operation on the compare results and a set of compare flags generated in a previous clock cycle of the instruction clock signal to generate the resultant compare flags.

38. The processor of claim 25, wherein the execution control unit is operable to executing one instruction having at least two branch control operators during each clock cycle of the instruction clock signal.

39. The processor of claim 25, wherein the execution control unit is operable to executing one conditional instruction during each clock cycle of the instruction clock signal.

40. The processor of claim 25, wherein the execution control unit is operable to repeating execution of a current instruction having a background mode operator during a next clock cycle of the instruction clock signal.

41. A protocol independent synchronous processor for processing network data, comprising:

an execution control unit synchronous with an instruction clock signal, the execution control unit operable to execute an instruction per clock cycle of the instruction clock signal;

an input interface synchronous with the instruction clock signal, the input interface operable to receive network data at a rate of one data word per clock cycle of the instruction clock signal; and

a plurality of configurable units synchronous with the instruction clock signal, the plurality of configurable units operable to process the received network data in real time under control of the execution control unit.

42. The protocol independent synchronous processor of claim 41 further comprising a plurality of configurable connections operable to interconnect the plurality of configurable units in real time under control of the execution control unit.

43. The protocol independent synchronous processor of claim 42 wherein the execution control unit is operable to configure the plurality of configurable units and the plurality of configurable connections in accordance with any selected network protocol of a multiplicity of predefined network protocols so as to configure the processor to process the received network data in real time in a manner consistent with the selected network protocol.

44. The protocol independent synchronous processor of claim 43 further comprising an instruction memory configured to store software instructions for the execution control unit, wherein the instructions define a procedure executable by the execution control unit, the procedure corresponding to the selected network protocol.

45. A protocol independent synchronous processor for processing network data, comprising:

an input interface for receiving the network data;

a plurality of software configurable units for processing a sequence of data words of the network data in real time, at a rate corresponding to a rate at which the network data is received at the input interface;

software configurable connections for interconnecting the plurality of software configurable units and input interface; and

a software execution unit, coupled to the plurality of software configurable units and software configurable connections, the software execution unit operable for configuring the plurality of software configurable units and software configurable connections in accordance with any selected network protocol of a predefined multiplicity of network protocols so as to configure the processor to process the received network data in real time in a manner consistent with the selected network protocol.